REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-20 are currently pending, Claims 1, 3-5, and 10 having been currently amended. The changes and additions to the claims do not add new matter and are supported by the originally filed specification, for example, on original Claim 10; page 13, line 5 to page 15, line 14; and Figure 1.

In the outstanding Office Action, Claims 1-5, 10-13, and 18-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Saito (U.S. Pub. No. 2002/0026553) in view of Texas Instruments ("Product Bulletin: Boundary-Scan Logic," hereafter "TI-BSL"); Claims 6-9 were rejected under 35 U.S.C. §103(a) as unpatentable over Saito in view of TI-BSL and Kumiko (Japanese Patent No. JP-9064811); and Claims 14-17 were rejected under 35 U.S.C. §103(a) as unpatentable over Saito in view of TI-BSL and Edwards et al. (U.S. Patent No. 6,684,348, hereafter "Edwards").

Amended Claim 1 recites, *inter alia*,

> a selection multiplex output block connected to the plurality of dedicated paths and configured to input the debug information via the dedicated paths, and output the inputted debug information; and
>
> at least two of the dedicated paths are provided for one of the plurality of function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with said one of the plurality of function blocks, as the debug information, from said one of the plurality of function blocks to the selection multiplex output block.

Applicants' Figure 1 shows a non-limiting embodiment of the features of Claim 1. In Figure 1, each function block (102, 104, 202, and 204) has two dedicated output paths connected to selection multiplex output block 403. The two paths for a function block are for transmitting respective input data and output data from the function block to the selection

multiplex output block (see specification, at page 14, lines 6-9). Advantageously, this feature allows each function block to continue to output the debug information in an arbitrary size including input data and/or output data to the outside of the signal processor serially from an arbitrary function block. Thus, a large amount of information required for debugging can be outputted regardless of a limited amount of a memory provided inside or outside a function block (see specification, at page 15, lines 15-21).

Applicants respectfully submit that the combination of Saito and TI-BSL fails to disclose or suggest these features of amended Claim 1.

Saito describes a method for monitoring regions in a processor circuit for bugs. Saito shows in Figs. 4-9, and 11 that functional blocks 21 send and receive signals outside the circuit through selection means 30 or through signal selection circuit 32 (see para. [0032] of Saito).

The Office Action acknowledges that Saito fails to disclose or suggest "at least two of the dedicated paths provided for one of the plurality of function blocks, said paths configured to transmit input data and output data associated with said one of the plurality of function blocks." (See Office Action at page 2). The Office Action relies on TI-BSL to remedy the deficiencies of Saito with regards to Claim 1. (See Office Action at pages 2-3, citing page 3 of TI-BSL).

TI-BSL is directed towards boundary-scan logic technology. The figure shown on page 3 of TI-BSL shows a core logic unit that is to be tested within the boundary-scan architecture. Boundary-scan register cells (BSCs) are interconnected between input/output pins and the core logic unit (see page 3 of TI-BSL, sixth full paragraph). During normal operations, input and output signals pass freely through the BSCs from a normal data input to the normal data output. When boundary test mode is entered, the BSCs operate to allow test stimulus data to be input from the test data input (TDI) pin and into the core logic unit and

output to the test data output (TDO) pin. Thus, the BSCs create an architecture that allows bypassing of normal input/output signals so that test stimulus data can be transmitted through the core logic unit and output to the TDO for inspection.

The Office Action takes the position that the boundary-scan architecture described by TI-BSL corresponds to "at least two of the dedicated paths provided for one of the plurality of function blocks, said paths configured to transmit input data and output data associated with said one of the plurality of function blocks." The path formed by the TDI line described in TI-BSL is actually transmitting test stimulus ***into*** the core logic unit as discussed above. In other words, the TDI line described in TI-BSL is providing test input data to the core logic unit. However, TI-BSL does not describe two dedicated paths transmitting input and output data associated with a function block ***from*** the function block to a multiplex block.

Thus, TI-BSL fails to disclose or suggest "at least two of the dedicated paths are provided for one of the plurality of function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with said one of the plurality of function blocks, as the debug information, from said one of the plurality of function blocks to the selection multiplex output block," as defined by amended Claim 1.

Therefore, TI-BSL fails to remedy the deficiencies of Saito with regards to amended Claim 1.

Thus, Applicants respectfully submit that amended Claim 1 (and all associated dependent claims) patentably distinguishes over Saito and TI-BSL, either alone or in proper combination.

Kumiko and Edwards have been considered but fail to remedy the deficiencies of Saito and TI-BSL with regards to amended Claim 1.

Therefore, it is respectfully submitted that amended Claim 1 (and all associated dependent claims) patentably distinguish over Saito, TI-BSL, Kumiko, and Edwards, either alone or in proper combination.

Consequently, in light of the above discussion and in view of the present amendment, the outstanding grounds for rejection are believed to have been overcome. The present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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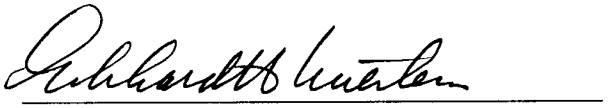

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